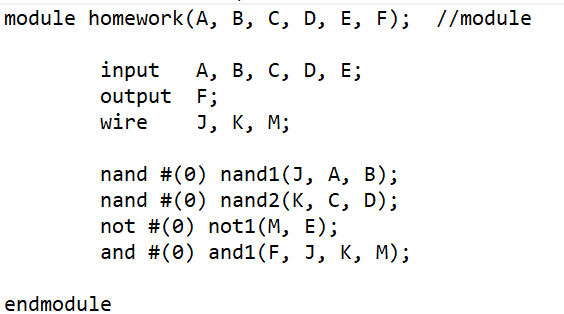
數位邏輯設計

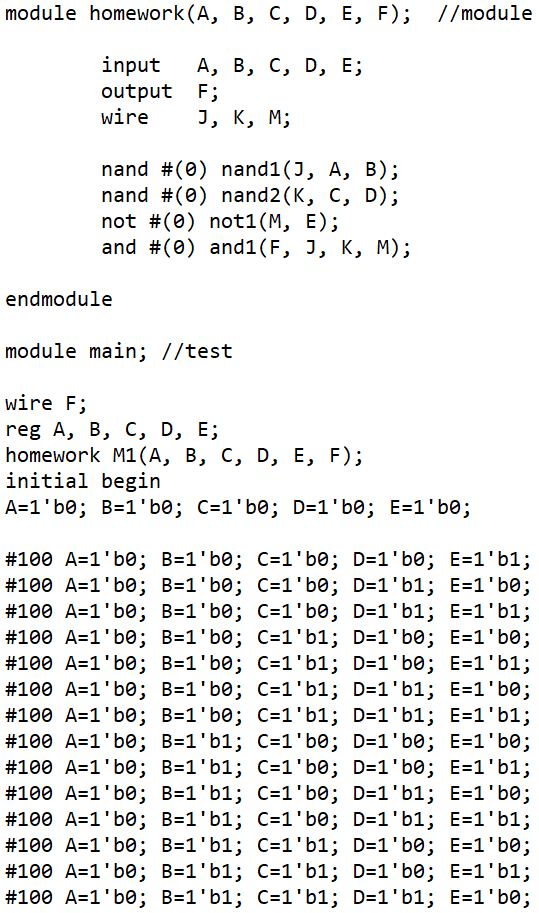
姓名：王蔚 學號：B10501109 作業：Circuit 4

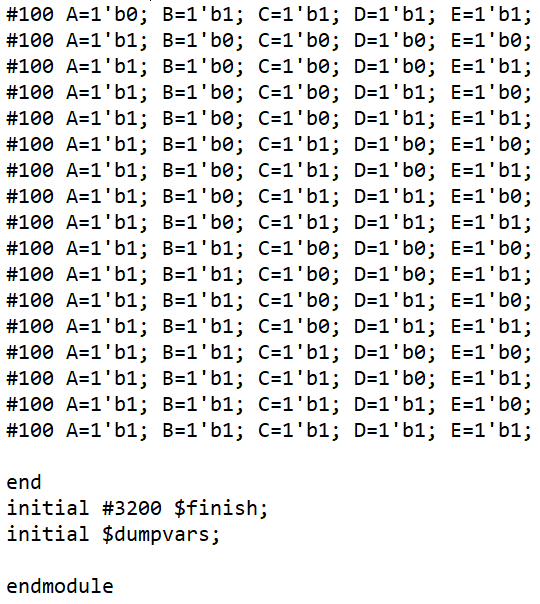
Part I

Verilog模組原始碼



Part II: 模擬測試原始碼 (分兩張圖 兩張圖中間有留白請見諒)





Part III:

電路圖簡化後

其真值表如下圖；

|  |  |
| --- | --- |
| ABCDE | F |
| 00000 | 1 |
| 00001 | 0 |
| 00010 | 1 |
| 00011 | 0 |
| 00100 | 1 |
| 00101 | 0 |
| 00110 | 0 |
| 00111 | 0 |
| 01000 | 1 |
| 01001 | 0 |
| 01010 | 1 |
| 01011 | 0 |
| 01100 | 1 |
| 01101 | 0 |
| 01110 | 0 |
| 01111 | 0 |
| 10000 | 1 |
| 10001 | 0 |
| 10010 | 1 |
| 10011 | 0 |
| 10100 | 1 |
| 10101 | 0 |
| 10110 | 0 |
| 10111 | 0 |
| 11000 | 0 |
| 11001 | 0 |
| 11010 | 0 |
| 11011 | 0 |
| 11100 | 0 |
| 11101 | 0 |
| 11110 | 0 |
| 11111 | 0 |

發現在ABCDE = 00001, 10101, 10111, 11010, 11101, 11111等六種狀態下輸出為True，符合波形模擬結果

